

Vital System Processor 2 (VSP2) Printed Circuit Board

With a 250 millisecond cycle time, the integrated Vital Processor Interlocking (iVPI®) Vital System Processor 2 (VSP2) reliably and safely processes all vital safety functions including Vital logic processing, Vital input and output control, and manages Vital data communications. VSP2 processes up to 9000 Vital Boolean expressions during each cycle to support application logic for complex train control applications – including Vital blocking and track circuit sequence-checking.



iVPI® Vital System Processor 2 Printed Circuit Board

Key Benefits

- 9000 Vital Boolean expressions processing
- 320 Vital inputs processed from up to 20 Direct Input (DI) boards
- 320 Vital outputs processed from up to 40 Vital output boards
- 1000 permanent software timers

Network Communications to Support Complex Interlockings

The VSP2 is equipped with 2 configurable Ethernet ports for network redundancy to ensure continued communications in the event one network goes down.

- Two 10/100 Mbit application Ethernet devices
- Supports redundant network configurations using KB Signaling's Vital Serial Over Ethernet 2 (VSoE2) and DigiSAFE and FSFB/2 protocols
- Web browser diagnostics
- One 10/100 MBit Ethernet RJ45 port (front panel) for diagnostics using the web interface



General Description

The iVPI® Vital system functions are solely performed by the VPS2 Board, which fully completes thousands of fail-safe microprocessor operations four times every second. VSP2 ensures control of iVPI vital inputs and outputs (I/O), manages the duration of timed events and vital signaling rules, and communicates vital and non-vital messages to other subsystems. Its high processing capacity supports complex train control applications. These applications include Automatic Train Protection (ATP) to Vitally enforce train operation, Automatic Train Operation (ATO) by Vitally regulating train speeds and station stopping and Automatic Train Supervision (ATS) to automatically route trains. KB Signaling's Numerically Integrated Safety Assurance Logic™ (NISAL), ensuring the iVPI system operates in a fail-safe manner.

Vital and non-vital iVPI subsystems operate independently, linked only through an optional application data exchange channel used to communicate non-vital information.

Customer Benefits

Vital Software Timers Reduce Costs

During each processing cycle, VSP2 processes up to 1120 Vital timers, including 1000 Permanently Programmable Vital Timers (PPVT) and 120 Field Settable Software Vital Timers (FSSVT). FSSVT are programmed using a web-based tool and when updated, do not require iVPI application logic to be recompiled.

Scalable Vital Interlocking Solution

The iVPI requires only a single VSP2 board in each system. Up to 2 expansion subracks can be added to each iVPI system to increase the I/O VSP2 manages. iVPI routes VSP2 communications to these expansion subracks via a ribbon cable connecting it to the Bus Expansion Boards, simplifying the hardware required to upscale system sizing.

Vital and Non-vital Application Processing

The VSP2 board design includes two application processors: one Vital processor and one Non-Vital Subsystem Module (NVSM).

The VSP2 Vital application processor processes Vital I/O, Boolean equations and protocols.

The VSP2 NVSM processes non-vital Application Boolean parameters, true/false values and advanced programming features, including integer arithmetic, program flow controls, predefined subroutines and arrays. A separate non-vital processor board is necessary only when RS232/422 links are required.

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Key Benefits

Event Recording

The VSP2 logs and time-date stamps user-specified signaling system events and health events. Real-time event recording is time-stamped to a resolution of one millisecond, making the need for external recording systems unnecessary. Up to 6.5 billion events can be recorded and stored for an unlimited time on a commonly-available 32GB Secure Digital High Capacity (SDHC) memory card. Events can be downloaded locally using the Maintenance Management System (MMS) or by authorized users through a web browser.



Reduced Redundancy Costs

The VSP2 reduces deployment costs of interlocking processor redundancy by using the same application programming for both – lowering the design, testing, commissioning and maintenance costs. Redundant systems use VSP2-to-VSP2 (V2V) point-to-point highspeed interfaces to exchange and compare vital application parameters. This comparison is performed every quarter-second by the VSP2 executive software to confirm that the two systems' applications states are the same, allowing for a seamless transfer.



The VSP2 is designed to support efficient and accurate troubleshooting. LED indications are easily visible from the front panel, providing critical information on the statuses of board health, Vital and non-vital processors serial channels and network links. Optionally, an Interface board equipped with two RJ-45, power and Vital Relay Driver (VRD) connections can be installed on the back of the VSP2 board.

Web-based and Local Diagnostics

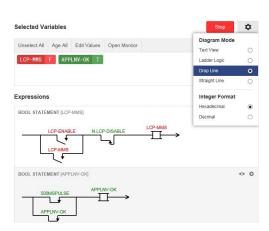
The VSP2 board's logic processor program memory incorporates a diagnostic program to test CPU operations and peripheral boards. It supports both local and remote access for diagnostic, configuration and maintenance activities. USB and Ethernet connections are accessible from the front of the VSP2 board for local access. Ethernet connections accessible from the back of the VSP2 board support remote access using either the web browser or the MMS – both provide real-time status of the logic states.

Refer to KB Signaling manual series P2521 for additional information.

Ordering Information

Board Assembly, iVPI, VSP2	31166-551-01
Board Assy, iVPI, VSP2, Interface P1	31166-557-01







KB Signaling

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